



P113SD Series 2.5 V CMOS Clock Oscillators

July 2007



- Pletronics' P113SD Series is a quartz crystal controlled precision square wave generator with a CMOS output.
- The P113SD series will directly interface TTL devices also.
- Greatly reduces RFI and EMI system sensitivity
- Minimizes RFI radiation, eases meeting FCC Class B emissions standards.
- Capable of driving up to 30pF capacitive loads
- Tube packaging is available.
- 70 to 135 MHz
- Full Size Thru-Hole DIP package
- Enable/Disable Function
- Disable function includes low standby power mode
- 3rd Overtone Crystals used
- Improved circuit to minimize oscillator issues such as multi-mode output signal.
- Low Jitter
- Has internal bypass capacitor on the Vcc lead
- 5x7 mm LCC ceramic oscillator inside

Pletronics Inc. certifies this device is in accordance with the RoHS (2002/95/EC) and WEEE (2002/96/EC) directives.

Pletronics Inc. guarantees the device does not contain the following:
 Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's
 Weight of the Device: 4.0 grams
 Moisture Sensitivity Level: 1 As defined in J-STD-020C
 Second Level Interconnect code: e1 or e2

Absolute Maximum Ratings:

Parameter	Unit
V _{CC} Supply Voltage	-0.5V to +7.0V
V _i Input Voltage	-0.5V to V _{CC} + 0.5V
V _o Output Voltage	-0.5V to V _{CC} + 0.5V

Thermal Characteristics

The maximum die or junction temperature is 155°C
 The thermal resistance junction to board is 120°C/Watt depending on the solder pads, ground plane and construction of the PCB.

Part Number:

P11	45	-3SD	ES	W	-85.0M	-30	-XX	Marking
Internal code or blank								
Output Load Capacitance Blank = 15pF maximum 30 = 30pF maximum - <100 MHz only								none
Frequency in MHz								<i>fff.fff</i> M
Supply Voltage V_{CC} W = 2.5V ± 10%								W, B, C or D
Enhanced Specifications (apply in the order shown) E = Temperature range -40 to 85°C S = Symmetry 45%/55% at 50% of V _{CC}								E S
Series Model								
Frequency Stability 45 = ± 50 ppm 44 = ± 25 ppm 20 = ± 20 ppm								5 4 2
Series Model								P3S

Part Marking:

PLE
P3Sxsss
fff.fff M
yywwaLF

Where: x = Frequency stability
 sss = Enhanced specification and voltage
 fff.fff = Frequency in MHz
 yywwa = Date code
 LF = Lead Free

Pletronics may ship the following combinations without notice (this is an enhanced specified device)

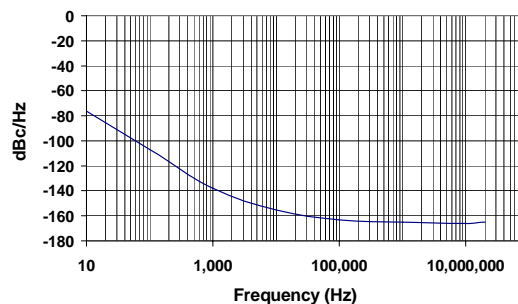
- 44 (25 ppm) stability parts when 45 (50 ppm) was ordered
- 20 (20 ppm) stability parts when 45 (50 ppm) or 44 (25 ppm) was ordered.
- E temperature range parts when extended was not ordered.
- S symmetry parts when 40/60% symmetry was ordered.

Pletronics may ship parts that are not marked for extended temperature range but were tested for extended temperature range, a Certificate of Conformance will accompany these parts.

Electrical Specification for 2.50V $\pm 10\%$ over the specified temperature range

Item	Min	Max	Unit	Condition
Frequency Range	70	135	MHz	
Frequency Accuracy "45"	-50	+50	ppm	For all supply voltages, load changes, aging for 1 year, shock, vibration and temperatures
"44"	-25	+25		
"20"	-20	+20		
Output Waveform	CMOS			
Output High Level	90	-	%	of V_{CC} (See load circuit)
Output Low Level	-	10	%	of V_{CC} (See load circuit)
Output Symmetry	40	60	%	at 50% point of V_{CC} (See load circuit) Standard
	45	55	%	for "S" option parts
Jitter	-	0.6	pS RMS	12 KHz to 20 MHz from the output frequency
	-	2.5	pS RMS	10 Hz to 1 MHz from the output frequency
Enable/Disable Internal Pull-up	50	-	Kohm	to V_{CC}
V disable	-	30	%	of V_{CC} applied to pad 1
V enable	70	-	%	of V_{CC} applied to pad 1
Output leakage $V_{OUT} = V_{CC}$	-10	+10	μA	Pad 1 low, device disabled
	$V_{OUT} = 0V$	-10	+10	
Standby Current I_{CC}	-	3	μA	Pad 1 low, device disabled
Enable time	-	100	nS	Time for output to reach a logic state
Disable time	-	100	nS	Time for output to reach a high Z state
Start up time	-	10	mS	Time for output to reach specified frequency
Operating Temperature Range	0	+70	$^{\circ}C$	Standard Temperature Range
	-40	+85	$^{\circ}C$	Extended Temperature Range "E" Option
Storage Temperature Range	-55	+125	$^{\circ}C$	

Typical phase-noise characteristics at 106.25MHz

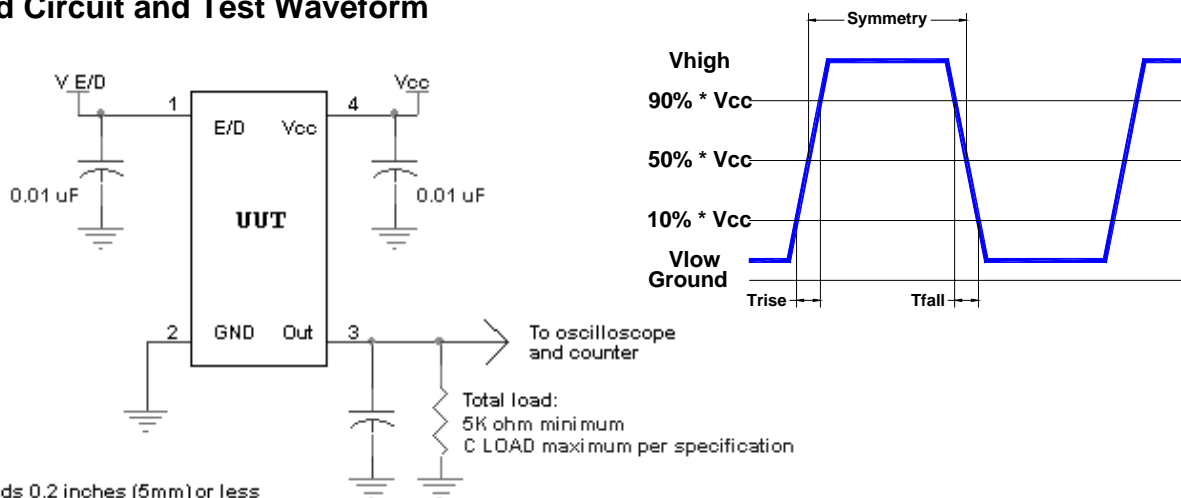


Electrical Specification for 2.50V $\pm 10\%$ over the specified temperature range

Item	Min	Typ	Max	Unit	Condition	
V_{OUT} High (V_{OH})	2.5	2.7	-	V	$V_{CC} = 2.97V, I_{OH} = +8$ mA	
V_{OUT} Low (V_{OL})	-	0.3	0.4	V	$V_{CC} = 2.97V, I_{OL} = -8$ mA	
Output T_{RISE} and T_{FALL}	-	1.0	3.0	nS	>110 MHz	$C_{LOAD} = 15$ pF 10% to 90% of V_{CC} See Load Circuit
	-	1.0	3.0	nS	>80 MHz and ≤ 110 MHz	
	-	2.0	4.0	nS	≤ 80 MHz	
	-	2.5	4.0	nS	>110 MHz	$C_{LOAD} = 30$ pF 10% to 90% of V_{CC} See Load Circuit
	-	2.5	4.0	nS	>80 MHz and ≤ 110 MHz	
	-	3.5	6.0	nS	≤ 80 MHz	
V_{CC} Supply Current (I_{CC})	-	25	60	mA	>110 MHz	$C_{LOAD} = 15$ pF
	-	20	50	mA	>80 MHz and ≤ 110 MHz	
	-	15	40	mA	≤ 80 MHz	
	-	38	70	mA	>110 MHz	$C_{LOAD} = 30$ pF
	-	31	60	mA	>80 MHz and ≤ 110 MHz	
	-	20	45	mA	≤ 80 MHz	

Specifications with Pad 1 E/D open circuit

Load Circuit and Test Waveform



Reliability: Environmental Compliance

Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002, Condition A
Vibration	MIL-STD-883 Method 2007, Condition A
Solderability	MIL-STD-883 Method 2003
Thermal Shock	MIL-STD-883 Method 1011, Condition A






ESD Rating

Model	Minimum Voltage	Conditions
Human Body Model	1500	MIL-STD-883 Method 3115
Charged Device Model	1000	JESD 22-C101

Package Labeling

Label is 1" x 2.6" (25.4mm x 66.7mm)
Font is Courier New
Bar code is 39-Full ASCII

Label is 1" x 2.6" (25.4mm x 66.7mm)
Font is Arial

P/N:		
	P1145-3SDW-125.0M	
Customer P/N:		
	12345678	
Qty:		D/C 
	1000	0502A6

<p>Pb Free</p> <p>2nd LvL Interconnect Category=e1</p> <p>Max Safe Temp=280C for 15s (Wave solder only) Max Safe Temp=245C for 10s (Reflow only)</p>

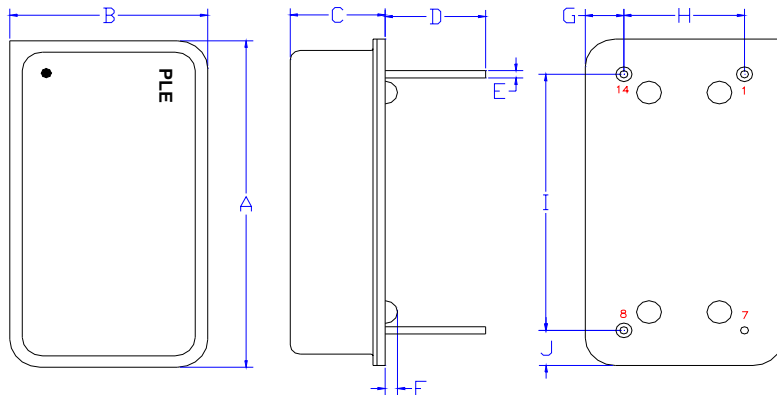
<p>Pb Free</p> <p>2nd LvL Interconnect Category=e2</p> <p>Max Safe Temp=280C for 15s (Wave solder only) Max Safe Temp=245C for 10s (Reflow only)</p>

PCB Mounting (typical for lead free processing)

Hand soldering is recommended.

Wave solder at 255°C to 280°C with maximum wave exposure of 15 seconds
Reflow solder maximum exposure of 245°C for 15 seconds
Soldering done in a nitrogen atmosphere enhances the solder joint quality.

Mechanical:



Cover:
Kovar
Electroless Nickel Plated
1 μinch (25 μm) typical
Resistance welded to base

Base:
Kovar
Glass to metal sealed leads

Label:
White Kapton with Black Letters
-or-
Blue Epoxy heat cure ink with laser
marked lettering

Pin 7 Connected to case

Not to scale

	Inches	mm
A	0.787 ±0.005	20.00 ±0.13
B	0.487 ±0.005	12.37 ±0.13
C	0.225 ±0.011	5.72 ±0.28
D ¹	0.250	6.35
E ¹	0.020	0.51
F ¹	0.031	0.79
G ¹	0.094	2.37
H ¹	0.300	7.62
I ¹	0.600	15.24
J ¹	0.094	2.37

¹ Nominal dimension

Pad	Function	Note
1	Output Enable/Disable	When this pad is not connected the oscillator shall operate. When this pad is logic low the output will be inhibited (high impedance state.) Recommend connecting this pad to V _{CC} if the oscillator is to be always on.
7	Ground (GND)	
8	Output	
14	Supply Voltage (V _{CC})	Recommend connecting appropriate power supply bypass capacitors as close as possible.

Layout and application information



For Optimum Jitter Performance, Pletronics recommends:

- a ground plane under the device
- no large transient signals (both current and voltage) should be routed under the device
- do not layout near a large magnetic field such as a high frequency switching power supply
- do not place near piezoelectric buzzers or mechanical fans.



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